What is claimed is:

1. A method for verifying a memory array, the method comprising:
selecting an addressable block of memory cells;
identifying an address of a memory cell in the addressable block, wherein the address is greater than a lowest address of the selected addressable block; and
performing an erase verification of the memory cell.

2. The method of claim 1 where identifying the address comprises reading contents of an address register.

3. The method of claim 2 further comprises copying the contents of the address register to an address counter.

4. The method of claim 3 further comprises:

sequentially incrementing contents of the address counter after the contents of the address register has been copied; and

sequentially reading additional memory cells of the addressable block.

5. The method of claim 1 and further including performing an erase operation prior to verifying the memory array, the erase operation comprising:
performing a pre-program operation on the addressable block of memory cells;

applying an erase pulse to the block of memory cells;

performing a first erase verification operation on a first sub-block of the block of memory cells;
terminating the erase verification of the first sub-block; and
recording an address of a memory cell in the first sub-block when the erase verification of the first sub-block is terminated.

6. A non-volatile memory device comprising:

a plurality of blocks of memory each having groups of memory sub-blocks, each memory sub-block comprising a plurality of memory cells and an erase indication register; and

control circuitry coupled to the plurality of blocks of memory, the control circuitry capable of executing an erase verification operation comprising selecting an addressable block of memory cells, identifying an address of a memory cell in the addressable block, wherein the address is greater than a lowest address of the selected addressable block, and performing an erase verification of the memory cell.

7. The device of claim 6 wherein the control circuitry is a state machine.

8. A memory system comprising:

a processor that generates control signals; and

a non-volatile memory device coupled to the processor, the device comprising:

a plurality of blocks of memory each having groups of memory sub-blocks, each memory sub-block comprising a plurality of memory cells and an erase indication register; and

control circuitry coupled to the plurality of blocks of memory, the control circuitry capable of executing an erase verification operation in response to the processor control signals, the operation comprising selecting an addressable block of memory cells, identifying an address of a memory cell in the addressable block, wherein the address is greater than a lowest address of the selected addressable block, and performing an erase verification of the memory cell.